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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,955	12/20/2001	Satoru Mayuzumi	NEC 01FN061	4588

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,955	MAYUZUMI, SATORU	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31,32,34,35,37,38 and 40-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31,32,34,35,37,38 and 40-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 31, 32, 34, 35, 37, 38 and 40-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 31 and 32 recite unclear limitations of "a first transistor which is connected between a first power supply line and a first node and has a gate that is connected to a second node without connection to a first node; a second transistor which is connected between a second power supply line and said second node and has a gate that is connected to a first node without connection to said second node; an extended gate wiring that is extended from the gate electrode of said first transistor up to the vicinity of a diffusion layer of said second transistor; and a common contact formed across the extended gate wiring and the diffusion layer of said second transistor." First, a transistor cannot be connected *between* a power supply and a node. Note that a transistor has to be connected to power (Vcc) or a node. Second, the instant invention does not disclose a second power line for the second transistor. Third, the gate wiring of the first transistor is not extended up *to the vicinity of a diffusion layer* of said second transistor. The gate wiring of the first transistor is connected to the diffusion layer of said second transistor.

It appears that the pending claims recite a circuit diagram in Figure 3A of the instant invention. And it is pointed out that Figure 3A of the instant invention is merely a configuration

to depict wiring connections between the transistors, and this configuration can be drawn in different ways still describing the same circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (US 5231038), hereinafter Yamaguchi in view Wu (US 5151374).

Regarding claim 31, insofar as understood, Fig. 1L of Yamaguchi shows a semiconductor device comprising:

a semiconductor substrate (41);

a gate insulating film (48) formed on said semiconductor substrate;

a gate electrode (52) formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion;

a side wall (44) formed on a side surface of the gate electrode so as to be covered behind the visor portion of the gate electrode;

wherein the visor portion has no overhang with respect to the sidewall.

Fig. 1L of Yamaguchi shows substantially an entire claimed structure of the device except "a first transistor which is connected between a first power supply line and a first node

and has a gate that is connected to a second node without connection to a first node; a second transistor which is connected between a second power supply line and said second node and has a gate that is connected to a first node without connection to said second node; an extended gate wiring that is extended from the gate electrode of said first transistor up to the vicinity of a diffusion layer of said second transistor; and a common contact formed across the extended gate wiring and the diffusion layer of said second transistor." Fig. 1 of Wu shows a circuit diagram which is identical to Fig. 3A of the instant invention, therefore having the identical wiring connection to the one recited in the instant invention.

It would have been obvious to one of ordinary skill in the art at the time of the invention made to utilize the teachings of Wu to the device of Yamaguchi in order to build a recited circuit configuration of SRAM since such a SRAM configuration is well known and readily available.

Regarding claim 42, Fig. 1 of Wu shows the diffusion layer is also a diffusion layer of a source a drain/source of a third transistor. In addition, it is obvious/ well known in the art that a configuration for a memory cell transistor has a common source /drain.

Claims 34, 37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi and Wu as applied to claim 31 above, and further in view of Satoh et al. (US 5834817), hereinafter Satoh.

Regarding claim 34, the combined teachings of Yamaguchi and Wu show substantially the entire claimed structure except "the gate electrode comprises a lower part substantially constant in the length along said gate length direction." Fig. 4D of Satoh shows a gate structure

which is identical to the pending claim showing the lower part of the gate is constant in the length along the gate length direction.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the shape of the gate of Yamaguchi and Kim with the teaching of Satoh in order to accommodate an obvious design variation of the gate shape as shown Figures 4C-4F of Satoh. Also, note that the lower portion of the gate of Yamaguchi can read *substantially constant*. The reference of Satoh is introduced only to show that a shape of the gate recited in the instant invention is one of various shaped gate known in the art. Therefore, it would have been obvious matter of design choice since such a modification would have involved a mere change in the shape of a component. A change in shape is generally recognized as being within the level of ordinary skill in the art. *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claim 37, Fig. 1L of Yamaguchi shows the side wall is formed on both a side surface of the upper part and a side surface of the lower part. It would be also obvious that the sidewalls of the modified gate structure with Satoh's teaching (Fig. 4D) would be formed only below the visor portion to utilize the self-alignment process of the sidewall formation.

Regarding claim 40, Fig. 1L of Yamaguchi shows a side surface of the upper part forms a tapered slope.

Claims 32, 35, 38, 41 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iguchi et al. (US 5734185), hereinafter Iguchi in view of Satoh and Wu

Regarding claim 32, Fig. 1(a) of Iguchi shows a semiconductor device comprising;

a semiconductor substrate (1);

a gate insulating film (17) on said semiconductor substrate;

a gate electrode (19) formed on said gate insulating film and having a portion increasing upward in the length along a gate length direction, said gate electrode further having a visor portion; and

a side wall (16; 16a, 15, 3, 2) formed on a side surface of the gate electrode so as to be covered behind the visor portion of the gate electrode, said side wall (16; 15, 3) being formed of a lamination of at least two different insulation films having different etching properties (col. 13, lines 24-25).

Iguchi shows most aspect of the instant invention except the visor portion without overhang. Fig. 4D of Satoh shows a gate structure which is identical to the pending claim.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the shape of the Iguchi's gate with the teaching of Satoh in order to accommodate an obvious design variation of the gate shape as shown Figures 4C-4F of Satoh. Therefore, it would be also obvious that the sidewalls of the modified Iguchi's gate structure would be formed only below the visor portion to utilize the self-alignment process of the sidewall formation.

The combined teachings of Iguchi and Sato show substantially an entire claimed structure of the device except "a first transistor which is connected between a first power supply line and a first node and has a gate that is connected to a second node without connection to a first node; a second transistor which is connected between a second power supply line and said second node and has a gate that is connected to a first node without connection to said second node; an extended gate wiring that is extended from the gate electrode of said first transistor up to the vicinity of a diffusion layer of said second transistor; and a common contact formed across the extended gate wiring and the diffusion layer of said second transistor." Fig. 1 of Wu shows a

circuit diagram which is identical to Fig. 3A of the instant invention, therefore having the identical wiring connection to the one recited in the instant invention.

It would have been obvious to one of ordinary skill in the art at the time of the invention made to utilize the teachings of Wu to the device of Iguchi and Sato in order to build a recited circuit configuration of SRAM since such a SRAM configuration well known and readily available.

Regarding claim 35, Fig. 1(a) of Iguchi et al. show the gate electrode comprises a lower part substantially constant in the length along said gate length direction, and an upper part on said lower part increasing upward in the length along said gate length direction.

Regarding claim 38, Fig. 1(a) of Iguchi shows the side wall is formed on both a side surface of the upper part and a side surface of the lower part. It would be also obvious that the sidewalls of the modified Iguchi's gate structure with Satoh's teaching would be formed only below the visor portion to utilize the self-alignment process of the sidewall formation.

Regarding claim 41, Fig. 1(a) of Iguchi shows a side surface of the upper part forms a tapered slope.

Regarding claim 43, Fig. 1 of Wu shows the diffusion layer is a diffusion layer of a source a drain/source of third transistor. In addition, it is obvious/ as well known in the art that a configuration for a memory cell transistor has a common source /drain.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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